matter has been added or amendments made which narrow the scope of any elements of invention. Accordingly, claims 1-7 are pending in this application and are submitted for consideration.

The Title of the Invention was objected to for not being descriptive and clearly indicative of the invention to which the claims are directed. The Title of the Invention has been replaced herein with --SEMICONDUCTOR DEVICE HAVING ELECTRICAL DIVIDED SUBSTRATE--, which clearly describes the claimed invention. Accordingly, the Applicants request that the objection be withdrawn.

Claims 5-7 were rejected under 35 USC §112, second paragraph, as being indefinite. In particular, it was asserted that the phrase "and/or" renders the claim indefinite because it is unclear. However, in the response filed February 21, 2001, claims 5-7 were amended in order to overcome the same rejection. The CPA filed May 14, 2001 entered the Amendment of February 21, 2001. Attached hereto is a copy of the Amendment filed February 21, 2001 and the CPA. Thus, it appears that this rejection was included in the present Office Action in error. Accordingly, Applicants request that the rejection be withdrawn.

Claims 1-4 were rejected under 35 USC 102(b) as being anticipated by Kenichi et al. (JP Hei 04-61269(a)). Applicants respectfully traverse the rejection and submit that claims 1-4 recite subject matter not shown or described by Kenichi.

Claim 1, upon which claims 2-4 depend, defines a semiconductor device, which includes a lightly doped semiconductor substrate of a first conduction type, a buried semiconductor layer of a second conduction type formed in a first region of the semiconductor substrate, spaced from a surface of the semiconductor substrate, a

semiconductor region of the second conduction type extending from the surface of the semiconductor substrate to a peripheral portion of the buried semiconductor layer, and a semiconductor region of the first conduction type formed in the semiconductor substrate surrounded by the buried semiconductor layer and the semiconductor region of the second conduction type. The concentration of an impurity in the semiconductor region of the first conduction type is substantially equal to a concentration of an impurity in the semiconductor substrate.

As a result of the claimed configuration, the present invention has the nonobvious advantage that the semiconductor region of the first conduction type is free from any damage that could be caused by impurity ion implantation due to the fact that the semiconductor region of the first conduction type is only lightly doped with an impurity by ion implantation. See Specification page 9, line 15 - page 10, line 1, and page 26, lines 2-5. Consequently, a leak current from the capacitor through the junction between the source/drain diffused layer of the transistor of the cell unit and the first conduction type semiconductor region is small, and frequent rewriting operations for retaining a charge of the capacity are not necessary.

It was asserted in the Office Action that Kenichi shows a semiconductor device that includes a lightly doped semiconductor substrate (n-type substrate I) of a first conduction type and a semiconductor region (n-well 6) of the first conduction type. wherein a concentration of an impurity in the semiconductor region of the first conduction type is substantially equal to a concentration of an impurity in the semiconductor substrate. However, in Kenichi, the concentration of the impurity in the n-well 6 is not substantially equal to the concentration of the impurity in the n-type

substrate 1. In Kenichi, the n-well 6 is formed by implanting an n-type impurity in the n-type substrate 1. Therefore, the concentration of the impurity in the n-well 6 must be higher than the concentration of the impurity in the n-type substrate 1, and therefore, the n-well 6 is damaged by an n-type impurity ion implantation. Thus, Applicants submit that Kenichi fails to show each and every element of the claimed invention. Accordingly, Applicants request that the rejection be withdrawn and claims 1-4 be allowed.

Claims 5-7 were rejected under 35 USC 103(a) as being unpatentable over Kenichi in view of Applicants admitted prior art. It is admitted in the Office Action that Kenichi fails to show that the first semiconductor element and/or the second semiconductor element is a memory cell. It was asserted that it would have been obvious to combine figure 29A of the present invention with Kenichi in order to derive the present invention as defined by claims 5-7. Applicants respectfully traverse the rejection and assert that claims 5-7 recite subject matter which is neither shown nor suggested by any combination of the cited prior art.

As described above, in Kenichi, the concentration of the impurity in n-well 6 is not substantially equal to the concentration of the impurity in the n-type substrate 1, but must be higher. Therefore, in Kenichi, the n-well 6 is damaged by an n-type impurity ion implantation. Applicants admitted prior art fails to make up for this deficiency in Kenichi Furthermore, Applicants submit that if the memory cell of the Applicants admitted prior art is formed in the n-well 6 of Kenichi, then there will be a large leak current from a capacitor of the memory cell through the junction between the source/drain diffused layer and the n-well 6. Consequently, rewriting operations must be frequently

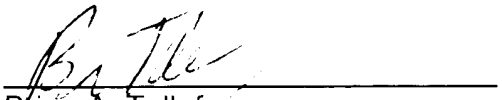
performed to maintain a charge of the capacitor, which increases power consumption. Therefore, there would have been no motivation to combine Kenichi and Applicants admitted prior art, and no combination of Kenichi or the Applicants admitted prior art show or suggest each and every feature of claims 5-7. Accordingly, Applicants request that the rejection be withdrawn and that claims 5-7 be allowed.

In view of the above remarks, the Applicants respectfully submit that each of claims 1-7 recite subject matter which is neither disclosed nor suggested in the cited prior art. Applicants submit that this subject matter is more than sufficient to render the claimed invention unobvious to a person of ordinary skill in the art. Applicants therefore request that each of claims 1-7 be found allowable, and this application passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not timely filed, the Applicants respectfully petitions for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account No. 01-2300.

Respectfully submitted,



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Enclosures
Copy of Amendment Filed February 21, 2001
Copy of CPA filed May 14, 2001
Marked-up Copy of the Amended Specification

MARKED UP COPY OF AMENDED SPECIFICATION

The Title of the Invention was amended as follows:

SEMICONDUCTOR DEVICE [AND METHOD FOR FABRICATING THE SAME]

HAVING ELECTRICAL DIVIDED SUBSTRATE